



Customer No. 22,852  
Attorney Docket No. 04329.3192

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:	)	
	)	
Hideshi MIYAJIMA et al.	)	
	)	Group Art Unit: 1765
Application No.: 10/726,678	)	
	)	Examiner: Not assigned
Filed: December 4, 2003	)	
	)	
For: <b>METHOD OF</b>	)	
<b>MANUFACTURING</b>	)	
<b>SEMICONDUCTOR DEVICE</b>	)	

**Commissioner for Patents**  
**P.O. Box 1450**  
**Alexandria, VA 22313-1450**

Sir:

**INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)**

Pursuant to 37 C.F.R. §§1.56 and 1.97(b), applicants bring to the Examiner's attention the documents listed on attached Form PTO-1449. Copies of the listed documents are attached. Applicants respectfully request that the Examiner consider the documents listed on attached Form PTO-1449 and indicate that they were considered by making an appropriate notation on this form.

This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits for the above-referenced application.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and applicants determine

that the cited documents do not constitute "prior art" under United States law, applicants reserve the right to present to the Office the relevant facts and law regarding the appropriate status of such documents. Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

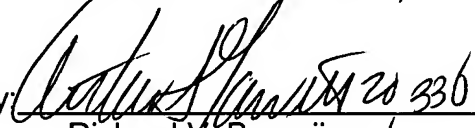
If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

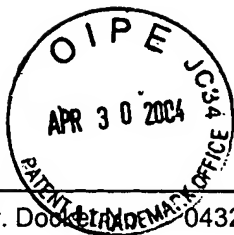
FINNEGAN, HENDERSON, FARABOW,  
GARRETT & DUNNER, L.L.P.

Dated: April 30, 2004

By

  
Richard Y. Burgujian /  
Reg. No. 31,744

Enclosures  
RVB/FPD/dvg



## INFORMATION DISCLOSURE CITATION

Atty. Docket No. 04329.3192	Application No. 10/726,678
Applicant Hideshi MIYAJIMA et al.	
Filing Date December 4, 2003	Group: 1765

## U.S. PATENT DOCUMENTS

Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate

## FOREIGN PATENT DOCUMENTS

Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Higashi, K. et al., "A Manufacturable Copper/Low-k SiOC/SiCN Process Technology for 90nm-node High Performance eDRAM", Proceeding of the IEEE2002 International Interconnect Technology Conference, pp. 15-17, (June 2002).
	Fayolle, M. et al., "Intergration of Cu/SiOC in Dual Damascene interconnect for 0.1µm technology using a new SiC material as dielectric barrier", Proceeding of the IEEE2002 International Interconnect Technology Conference, pp. 39-41, (June 2002).
	Kim, T.S. et al., " Intergration of Organosilicate Glasses (OSGs) In High Performance Copper Interconnects", Advanced Metallization Conference 2001, pp. 25-31, (October 2001)
	Fayolle, M. et al., "Overcoming resist poisoning issue during Si-O-C dielectric integration in Cu Dual Damascene interconnect for 0.1µm technology", pp. 509-513, (October 2001).
	Lin, J.C. et al., "Via First Dual Damascene Integration of nanoporous Ultra Low-k Material", IEEE2002 International Interconnect Technology Conference, pp. 48-50, (June 2002).

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce